Computer System Architecture  
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Tutorial 2:

1. A benchmark program is run on an 80 MHz processor. The executed program consists of 100,000 instruction execution, with the following instruction mix and clock cycle count:

|  |  |  |
| --- | --- | --- |
| Instruction Type | Instruction Count | Cycle per Instruction |
| Integer Arithmetic | 45000 | 1 |
| Data Transfer | 32000 | 2 |
| Floating Point | 15000 | 2 |
| Control Transfer | 8000 | 2 |

Determine the effective CPI, MIPS rate, and execution time for this program

Clock Rate : 80 MHz  
Instruction Count: 100 000

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction Type | Instruction Count | Frequency (%) | Cycle per Instruction | CPI \* F | %Time |
| Integer Arithmetic | 45000 | 45% | 1 | 0.45 | 29% |
| Data Transfer | 32000 | 32% | 2 | 0.64 | 41% |
| Floating Point | 15000 | 15% | 2 | 0.30 | 20% |
| Control Transfer | 8000 | 8% | 2 | 0.16 | 10% |
| Total |  | 100% |  | 1.55 | 100% |

CPI (Average number of cycles per instruction) = 1.55  
Execution time(CPU time) = Instruction count \* CPI/clock rate   
= 100 000 \* 1.55 / 80\*10^6   
= 1.9375\*10^-3s  
MIPS rate = Instruction count / (Execution time \* 10^6)   
= 100 000 / (1.9375\*10^-3 \*10^6)   
= 5.16

1. The performance of a 100MHz microprocessor P is measured by executing 10,000,000 instruction of benchmark code, which is found to take 0.25s. What are the values of CPI and MIPS for this performance experiment? Is P likely to be superscalar?

Clock Rate: 100 MHz  
Instruction Count: 10,000,000  
CPU Time: 0.25s  
CPI = CPU time \* (clock rate) / (Instruction count) = 0.25 \* 100^6 / 10^6 = 2.5  
MIPS = Instruction count/ (Execution time \* 10^6) = 10^6 / (0.25 \* 10^6) = 4  
P is not superscalar (The ability to issue more than one instruction in every processor clock cycle), as each cycle took 1\*10^-8s (1/100\*10^6) and the total time is 0.25s, therefore there is 25\*10^6 (0.25/ 1\*10^-8) cycles for 10^6 instructions.

1. Suppose that a single-chip microprocessor P operating at clock frequency of 50MHz is replaced by a new model P’, which has **the same architecture** as P but has a clock frequency of 75MHz.
   1. If P has a performance rating of p MIPS for a particular benchmark program Q, what is the corresponding MIPS rating p’ for P

75MHz / 50MHz = 1.5 -> 1.5p

* 1. P takes 250s to execute Q in a particular personal computer system C. On replacing P by P’ in C, the execution time of Q drops only to 220s. Suggest a possible reason for this disappointing performance improvement.

RC delay (Speed at which electrons flow limited by resistance and capacitance of metal wires connecting them).

1. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for a given benchmark program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?

Computer A faster than Computer B by 2 times. The shorter the clock cycle time, the higher the clock rate, the faster the computer.

1. A compiler designer is deciding between two codes for a particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B, and Class C, and they require one, two, and three cycles respectively.

First code has 5 instructions: 2 of A, 1 of B, and 2 of C.

Second code has 6 instructions: 4 of A, 1 of B, and 1 of C.

Which code is faster?

By how much?

What is the CPI for each code?

First code：  
Number of clock cycles: 2(1) + 1(2) + 2(3) = 10  
Instruction count = 5  
CPI = 10/5 = 2  
1 instruction need 2 clock cycles.

Second code：  
Number of clock cycles: 4(1) + 1(2) + 1(3) = 9  
Instruction count = 6  
CPI = 9/6 = 1.5  
1 instruction need 1.5 clock cycles.  
  
Second code is faster.  
Second code need lesser clock cycle for one instruction.   
Second code has lower CPI than first code.  
Second code faster than first code by 0.75 times. (1.5/2)